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衛星定位系統解調模組

P/N: SH-DSRM-1

All in Typical Values		SAW+LNA	Power Divider	SAW	Optional Attenuator	MAX2769
GPS Path	Gain/Loss	16	-3.25	-2.8	0	18
	Total Gain	16	12.75	9.95	9.95	27.95
	NF	1.5	3.25	2.8	0	1.4
	Total NF	1.5	1.585	1.728	1.728	1.839
Glonass Path	Gain/Loss	16	-3.25	-2.8	0	15
	Total Gain	16	12.75	9.95	9.95	24.95
	NF	1.5	3.25	2.8	0	2.7
	Total NF	1.5	1.585	1.728	1.728	1.975

Pin Assignment and Definition:

Pin	Definition	Description	Pin	Definition	Description
1	GND	Groud	20	+5V	Supply voltage for active antenna
2	SDI_1	GPS/GLS Data Digital Input	21	+3.2V	Main supply voltage
3	SCLK_1	GPS/GLS Clock Digital Input	22	GND	Groud
4	/CS_GPS	GPS Receiver Chip-Select Logic Input	23	ANT	RF input and +5v power supply for active antenna
5	/CS_GLS	GLS Receiver Chip-Select Logic Input	24	GND	Groud
6	Q1_GPS	GPS Q-Channel Voltage Outputs	25	VBAT	RTC Backup voltage
7	Q0_GPS	GPS Q-Channel Voltage Outputs	26	/IRQ1	RTC interrupt signals for alarm, timer, time update, and FOUT
8	I0_GPS	GPS I-Channel Voltage Outputs	27	/IRQ2	RTC C-MOS output / interrupt signals for timer and FOUT
9	I1_GPS	GPS I-Channel Voltage Outputs	29	CS_DAC	DAC Chip-Select Logic Input
10	Q1_GLS	GLS Q-Channel Voltage Outputs	31	CS_RTC	RTC Chip-Select Logic Input
11	Q0_GLS	GLS Q-Channel Voltage Outputs	32	SCLK_2	RTC/DAC Clock Digital Input
13	I0_GLS	GLS I-Channel Voltage Outputs	33	SDI_2	RTC/DAC Data Digital Input
15	I1_GLS	GLS I-Channel Voltage Outputs	34	SDO_2	RTC Data Digital Output
17	LD_GPS	GPS Lock-Detector CMOS Logic Output	35	LD_GLS	GLS Lock-Detector CMOS Logic Output
18	/SHDN_GPS	GPS Operation Control Logic Input	36	/SHDN_GLS	GLS Operation Control Logic Input
19	CLKOUT_GPS	GPS Reference Clock Output	37	CLKOUT_GLS	GLS Reference Clock Output

Mechanical Information:

